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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,612	03/14/2001	Thomas J. Pennello	MWI.003A	4549

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EXAMINER	
FERRIS III, FRED O	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 09/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/808,612	PENNELLO ET AL.	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/6/02, 2/11/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been presented for examination based on applicant's disclosure filed on 14 March 2001. Claims 1-24 have been rejected by the examiner.

Priority

2. Applicant's claim for priority based on provisional application number 60/189,521 filed on 15 March 2000 is acknowledged.

Information Disclosure Statement

3. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered. Specifically, page 6 of the specification lists "IEEE 1008-1987 IEEE Standard for Software Unit Testing", while page 10 lists "Operating Systems Principles", Brinch Hansen, Prentice Hall 1973, which have not been included in applicant's PTO-1449 IDS forms submitted 8 January 2002 and 11 February 2002.

Specification

*4. The disclosure is objected to because of the following informalities: Page 4, line 11 appears of have omitted the word "by" and should read "employed **by** the present invention". On page 3, line 27, the word "debig" is misspelled. Appropriate correction is required.*

Claim Interpretation

*5. Applicants are disclosing and claiming a method and apparatus for debugging distributed programs by identifying and initializing processes, executing a thread to control processes, and cycling between processes to monitor status. As currently written, the independent claims appear to be broadly drawn to subject matter that is commonly known in the art as **debugging of concurrent processes**. (See: "Debugging of Concurrent Processes", S. Grabner et al, IEEE 1066-6192/95, IEEE 1995, for example) Accordingly, the examiner has interpreted the claimed limitations relating to debugging of distributed programs as equivalent to techniques used in debugging of concurrent processes and has applied art rejections accordingly. (See: 102/103 rejections below)*

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 2-4, 14-18, and 22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification does not contain a written description of the hardware process of the invention commensurate in scope with these claims.

MPEP Section 2106 recites the following:

> *"An application will be deficient under 35 U.S.C. 112, first paragraph when the **written description is not adequate to identify what the applicant has invented**, or when the **disclosure does not enable one skilled in the art to make and use the invention as claimed without undue experimentation**. Deficiencies related to disclosure of the best mode for carrying out the claimed invention are not usually encountered during examination of an application because evidence to support such a deficiency is seldom in the record. Fonar Corp. v. General Electric Co., 107 F.3d 1543, 1548-49, 41 USPQ2d 1801, 1804 (Fed. Cir. 1997)."*

In this case, claims 2, 4, 14, 16, and 22 recite limitations relating to a simulation process and at least "one hardware process". While the specification makes reference to the fact that "certain portions" of the functionality "could be implemented in hardware if desired", (see page 9, line 2) there is no specific teaching or written description in the specification sufficient to allow one skilled in the art to realize a "hardware process" of the functionality of the embodiments of the claimed invention as disclosed in Figures 1-3 and recited on pages 8-14. The passages on specification page 13, line 8 to page 14, line 7 stating that "Hardware processes may be used when fast execution is desired" do not cure this deficiency since there is no specific written description of how these hardware processes would be implemented to achieve the desired fast execution. The

examiner therefore asserts that one skilled in the art would not know how to make and use the claimed "hardware process" from the written description contained in the specification without undue experimentation. Dependent claims 3, and 15-18 inherit the defect of the claims from which they depend.

Claim Rejections - 35 USC § 102

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1, 19, and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,516,460 issued to Merks et al.

Independent claims 1, 19 and 22 are drawn to:
Method for debugging distributed programs by:
Identifying processes
Initializing processes
Executing single thread of control among processes
Continuously switching between processes to obtain related status

Regarding independent claims 1, 19, and 23: Merks discloses debugging distributed programs over multiple processors, initializing processors, executing a control thread, switching between processes and obtaining status information. (Abstract, Background, CL1-L55 - CL4-L55, Fig. 1) For example, at column 9, line 5 Merks recites:

"the preferred embodiment of the present invention allows for simultaneous **debugging of multiple related processes** in a Windows NT and Windows 95 environment by having the call to WaitForDebugEvent( ) specify a **timeout period** and for **the loop to continuously poll for events from all debuggee processes**. The pseudocode is as follows:
// executing on **"special" debugger thread**
// DEBUG_EVENT debug_event;
for (;;)
// let all the debuggee processes run that are supposed to run"

Merks teaches the elements of the claimed limitations of the present invention (claims 1, 19 and 23) as follows:

- Method for debugging distributed programs: Merks discloses debugging processes in a distributed (multi) processor environment (Abstract, Background, CL4-L66, CL5-L5, 10, 15-35, CL11-L26). (Merks also discloses the storage medium for data CL11-L11)

- Identifying processes: Merks discloses (selectively) identifying among parent/child processes (CL5-L27-35, CL7-L39, CL10-L27-29, Fig. 4) during the debugging process.

- Initializing processes: Merks discloses initiating processes with initial parameters such as process information, code, variables, and indicators, (i.e. initializing the processes) and starting/restarting the debugging of processes (CL8-L44-51, CL11-L28).

- Executing single thread of control among processes: Merks discloses executing a thread (single) as part of the control process among processes (CL2-L7-11, CL9-L54-58).

- *Continuously switching between processes to obtain related status: Merks teaches continuously polling between processes in order to monitor the "status" of each pending debug process (CL9-L5-58).*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 2-18, 20-22, and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,516,460 issued to Merks et al in view of U.S. Patent 6,230,307 issued to Davis et al.

As previously cited above under 102(e) rejections, Merks teaches the elements of the limitations of independent claims 1, 19, and 23 as follows:

- Method for debugging distributed programs: Merks discloses debugging processes in a distributed (multi) processor environment (Abstract, Background, CL4-L66, CL5-L5, 10, 15-35, CL11-L26).

- Identifying processes: Merks discloses (selectively) identifying among parent/child processes (CL5-L27-35, CL7-L39, CL10-L27-29, Fig. 4) during the debugging process.

- Initializing processes: Merks discloses initiating processes with initial parameters such as process information, code, variables, and indicators, (i.e. initializing the processes) and starting/restarting the debugging of processes (CL8-L44-51, CL11-L28).

- Executing single thread of control among processes: Merks discloses executing a thread (single) as part of the control process among processes (CL2-L7-11, CL9-L54-58).

- Continuously switching between processes to obtain related status: Merks teaches continuously polling between processes in order to monitor the "status" of each pending debug process (CL9-L5-58). Merks polls to monitor the status of process information, code, variables, and indicators (CL8-L44-51, CL11-L28) in the debugging process.

However, Merks does not explicitly disclose the limitations of dependent claims 2-4 relating to:

- *simulation process*
- *hardware process*
- *analyzing status for errors*
- *defining object classes*
- *defining object subclasses for hardware and simulation processes*

Regarding dependent claims 2-4: Davis teaches the elements of the limitations of independent claims 2-4 as follows:

- *simulation process: Davis discloses the simulation (emulation) for both a* ***hardware and software*** *realization of circuit (object) elements (Abstract, CL1-L25-55, CL4-L 51-58, CL24-L16-18, Figs. 1, 6 and 9).*
- *hardware process: As noted above, Davis discloses the simulation (emulation) for both a* ***hardware and software*** *realization of circuit (object) elements (Abstract, CL1-L25-55, CL4-L 51-58, CL24-L16-18, Figs. 1, 6 and 9).*
- *analyzing status for errors: Davis discloses determining the status (i.e. analyzing status) of various object elements and detecting and responding to the occurrence of errors. (CL12-L23-33, Fig. 17, CL42-L49) (Merks discloses monitoring status as noted above)*
- *defining object classes: Davis discloses defining hardware object classes for emulated (simulated) circuit element (CL9-L54-67, CL10-L1-39, Figs. 11, 12)*
- *defining object* ***subclasses*** *for hardware and simulation processes: Davis further discloses defining subclasses for the hardware simulation (emulation) processes (CL11-L43-56, CL9-L5-24, Fig. 15)*

Merks further does not explicitly disclose the additional limitations of dependent claims 5-13 relating to:

- *first instance variable controlling processes*
- *dynamically changing polling time of process based on status*
- *interface for defining/accessing library of hardware processes*
- *library includes extension instructions*
- *initializing hardware simulator processes*
- *dynamically loadable library*

Regarding dependent claims 5-14: Davis teaches the elements of the limitations of independent claims 5-14 as follows:

- *first instance variable controlling processes: Davis discloses using variables in the thread based scheduling and controlling of processes from an initial (first) state (CL3-L32-37, CL7-L56,CL9-L25-53, CL12-L15-23, Fig. 17).*
- *dynamically changing polling time of process based on status: Davis discloses the use of various primitives for setting parameters relating to dynamically scheduling/dispatching tasks which can effect (change) the scheduling (polling) time for process execution and management (CL12-L15-37). (Merks also discloses a variable rate polling time as noted above)*
- *interface for defining/accessing library of hardware processes: Davis discloses defining, accessing, and interfacing to a library of dynamically re-configurable hardware processes. (CL5-L52-64, CL6-L14-33, CL8-L39-64, Figs. 3, 4, 9)*
- *library includes extension instructions: Extension instructions are reserved processor instruction set by the processor manufacturer, and hence would have been an obvious feature to include in the library of hardware processes. (See applicant's specification page 7, line 5-12)*
- *initializing hardware simulator processes: Davis discloses beginning the thread controlled hardware simulation (emulation) process from a known initial (i.e. initialized) state. (CL9-L20-25, Fig 10)*
- *dynamically loadable library: Davis discloses a dynamically loadable and re-usable library (CL8-L54 to CL9-L5).*

Regarding independent claims 14, 20-22, and 24: In addition to the limitations previously addressed above, independent claims 14, 20-22, and 24 include additional limitations relating to "one hardware process", "heterogenous processors", and a distributed "multi-processing" environment. As noted above, Davis discloses the simulation (emulation) for ***hardware process*** *realization of circuit (object) elements (Abstract, CL1-L25-55, CL4-L 51-58, CL24-L16-18, Figs. 1, 6 and 9). Both Davis and Merks support heterogenous processors since the library of Davis includes hardware processes from various integrated circuit manufactures and Merks method of debugging concurrent processes is capable of operating on hardware from various manufacturers as also noted above. Both Davis and Merks disclose simulation (emulation) debugging in a distributed multi-processor environment. (See Davis: Fig. 8, and Merks: Abstract) Davis further discloses an apparatus (claim 24) capable of carrying out the processes of the claimed limitations (Fig. 4).*

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Merks relating to debugging distributed programs over multiple processors, with the teachings of Davis relating to simulation (emulation) of ***hardware processes*** *of library based circuit (object) elements, to realize the claimed invention. An obvious motivation exists since this area of technology is highly competitive with many techniques for debugging concurrent processes available in the market place (see Grabner Abstract/Conclusion, for example) Accordingly, a skilled artisan would have made an effort to become aware of what*

capabilities had already been developed in the market place and, hence, would have been motivated to modify the teachings of Merks with the teachings of Davis in order to reduce development time and cost.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 6,718,294 issued to Bortfeld teaches debugging concurrent processes in a multi-simulator environment.

"Debugging of Concurrent Processes", S. Grabner et al, IEEE 1066-6192/95, IEEE 1995, teaches debugging concurrent processes in a multi-simulator environment.

"A Concurrent Program Debugging Environment using Real-time Replay", E.H. Piak et al, IEEE 0-8186-8227-2/97, IEEE 1997, teaches debugging concurrent processes in a multi-simulator environment.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 703-305-9670 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 703-305-3900.

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